A Capacitor Voltage-Balancing Method for Nested Neutral Point Clamped (NNPC) Inverter

Kai Tian, Bin Wu, *Fellow, IEEE*, Mehdi Narimani, *Senior Member, IEEE*, Dewei (David) Xu, *Member, IEEE*, Zhongyuan Cheng, *Member, IEEE*, and Navid Reza Zargari, *Fellow, IEEE*

***Abstract*—A capacitor voltage-balancing method for a nested neutral point clamped (NNPC) inverter is proposed in this paper. The NNPC inverter is a newly developed four-level voltage-source inverter for medium-voltage applications with properties such as operating over a wide range of voltages (2.4–7.2 kV) without the need for connecting power semiconductor in series and high-quality output voltage. The NNPC topology has two flying capacitors in each leg. In order to ensure that the inverter can operate normally and all switching devices share identical voltage stress, the voltage across each capacitor should be controlled and maintained at one-third of dc bus voltage. The proposed capacitor voltage-balancing method takes advantage of redundancy in phase switching states to control and balance flying capacitor voltages. Simple and effective logic tables are developed for the balancing control. The proposed method is easy to implement and needs very few computations. Moreover, the method is suitable for and easy to integrate with different pulse width modulation schemes. The effectiveness and feasibility of the proposed method is verified by simulation and experiment.**

***Index Terms*—Capacitor voltage-balancing method, multilevel inverter, nested neutral point clamped (NNPC) inverter, voltage-source inverter.**

I. Introduction

MULTILEVEL inverters are very popular in medium-voltage power conversion and motor drives due to low voltage stress on switches, better harmonic performance, low switching frequency, and less switching losses [1]. The main multilevel topologies include neutral point clamped (NPC) inverter, flying capacitor (FC) inverter, cascaded H-bridge inverter, and modular multilevel converter [2]–[5].

A new multilevel topology, named nested neutral point clamped (NNPC) inverter shown in Fig. 1, is proposed in [6]. This topology is a combination of an FC topology with an NPC topology, which provides four levels in output voltage. In comparison with the four-level NPC inverter, the NNPC inverter has less number of diodes, and in comparison to four-level FC inverter, it has fewer capacitors [6]. All switches in the topology have the same voltage stress equal to one-third of dc-link voltage. The NNPC inverter can operate in a wide range of 2.4–7.2 kV without the need for connecting power devices in series. As can be seen from Fig. 1, the NNPC topology has two FCs in each leg. The voltage across each capacitor should be controlled and balanced at one-third of dc-link voltage ($V_{\rm dc}/3$) to ensure that the inverter can operate normally [6], [23]–[25].

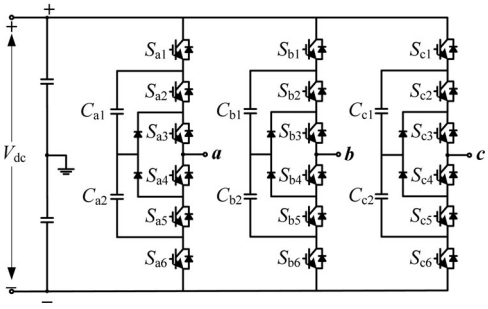


Fig. 1. Three phase nested neutral-point clamped (NNPC) inverter.

Several control techniques and modulation strategies including capacitor voltage-balancing methods have been developed in the literature for multilevel inverters [7]–[22]. The existing capacitor voltage-balancing methods are mainly developed for diode-clamped inverters [7]–[13], FC inverters [14]–[19], and modular multilevel inverters [20]–[22]. These methods are not suitable for the NNPC inverter due to different topology structures. The difference in the topology causes different behavior in capacitor voltages and thus need different voltage-balancing methods.

In order to control output voltage and get FC voltage balance, a space vector modulation (SVM) technique is presented in [6] for NNPC inverter. In this method, a cost function is defined based on the energy stored in capacitors. The cost function needs to be calculated repeatedly for each redundant switching state in every sampling period to find the best switching state to balance FC voltages. This method is complex and needs lots of calculations due to a large number of redundant switching states and introduces a considerable time delay in the actuation. At a low modulation index (less than 0.5), the number of switching redundancies goes very high, and therefore, the number of calculations will increase significantly. This computational delay can deteriorate the performance of the control system. Moreover, this method is not suitable for those modulation schemes without redundant three-phase switching states, such as sinusoidal pulse width modulation (SPWM).

In order to mitigate the aforementioned drawbacks, a new capacitor voltage-balancing method for the NNPC inverter is

Manuscript received February 10, 2015; revised April 15, 2015; accepted May 12, 2015. Date of publication June 1, 2015; date of current version November 16, 2015. Recommended for publication by Associate Editor C. N. M. Ho.

K. Tian, B. Wu, M. Narimani, and D. (D.) Xu are with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON M5B 2K3 Canada (e-mail: ktian@ee.ryerson.ca; bwu@ee.ryerson.ca; mnariman@ee.ryerson.ca; dxu@ryerson.ca).

Z. Cheng and N. R. Zargari are with the Medium Voltage R&D Department, Rockwell Automation Canada, Cambridge, ON N1R 5N9 Canada (e-mail: gcheng@ra.rockwell.com; nrzargari@ra.rockwell.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2015.2438779

TABLE I
PHASE VOLTAGES AND SWITCHING STATES IN NNPC INVERTER ($k = a, b, c$)

Phase voltage, v_k	Output Level, L_k	Phase switching states, S_k	Switching states of each device					
			S_{k1}	S_{k2}	S_{k3}	S_{k4}	S_{k5}	S_{k6}
$V_{\rm dc}/2$	3	3	1	1	1	0	0	0
$V_{\rm dc}/6$	2	2A	0	1	1	0	0	1
		2B	1	0	1	1	0	0
$-V_{\rm dc}/6$	1	1A	0	0	1	1	0	1
		1B	1	0	0	1	1	0
$-V_{\rm dc}/2$	0	0	0	0	0	1	1	1

proposed in this paper. In the proposed method, simple logic tables are developed to control the voltages of FCs. The proposed method has the following features:

1) the method is suitable for and can be easily integrated with different pulse width modulation (PWM) schemes such as SPWM and SVM, etc.;
2) the method uses simple logic tables, needs very few computations, and is easy to implement.

The effectiveness and feasibility of the proposed method is verified by simulation and experimental results.

II. OPERATION OF THE NNPC INVERTER AND BEHAVIOR ANALYSIS OF THE CAPACITOR VOLTAGES

A. Operation of the NNPC Inverter

The three-phase NNPC inverter is shown in Fig. 1. Each phase of the inverter consists of six switches, two clamping diodes, and two FCs. The voltages of the FCs should be kept at one-third of dc bus voltage ($V_{\rm dc}/3$) to generate four output levels in phase voltage and ensure that all the power switches share the same voltage stress. Table I shows the phase voltage v_k ($k = a, b, c$), output level L_k, as well as the corresponding phase switching state S_k. For each phase, the four distinct output voltages are $-V_{\rm dc}/2$, $-V_{\rm dc}/6$, $V_{\rm dc}/6$, and $V_{\rm dc}/2$, corresponding to the four output levels 0, 1, 2, and 3, respectively. The phase voltage is defined as the voltage at the output terminal of each phase with respect to the midpoint of dc bus. The relationship of v_k and L_k can be expressed as

$$v_k = (2L_k - 3)V_{\rm dc}/6. \tag{1}$$

As can be seen from Table I, levels 0 and 3 have no redundant switching state, while levels 1 and 2 both have two redundant switching states. The redundant switching states for level 1 are 1A [001101] and 1B [100110]. The two redundant switching states generate the same output voltage $-V_{\rm dc}/6$ with different switches ON and OFF. For level 2, the two redundant switching states are 2A [011001] and 2B [101100], generating the same phase voltage $V_{\rm dc}/6$ with different switches ON and OFF.

B. Behavior Analysis of the Capacitor Voltages in the NNPC Inverter

Different redundant switching states have different impacts on FC voltages. The analysis of this impact is illustrated in Fig. 2, in which the six overall switching states are analyzed.

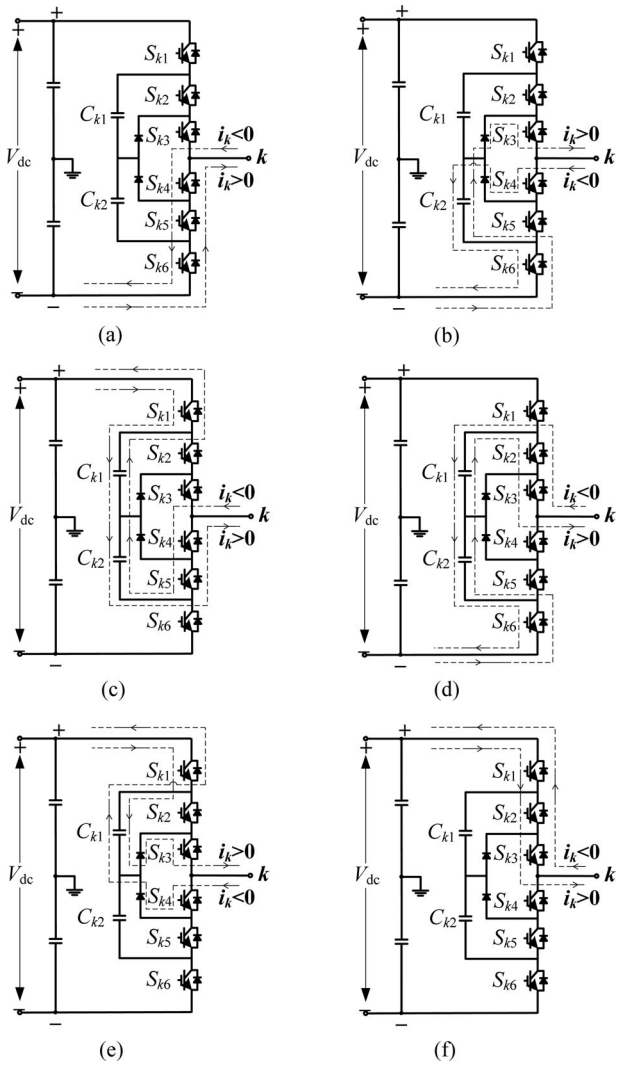


Fig. 2. Impacts of different phase switching states and phase current on capacitor voltages in NNPC inverter. (a) Switching state 0. (b) Switching state 1A. (c) Switching state 1B. (d) Switching state 2A. (e) Switching state 2B. (f) Switching state 3.

In Fig. 2, C_{k1} and C_{k2} are the two series FCs in the phase k ($k = a, b, c$), whose voltages are denoted by V_{Ck1} and V_{Ck2}. The behavior of the capacitor voltages depends on the switching state S_k and the phase current i_k.

As shown in Fig. 2(a) and (f), the switching states 0 and 3 (corresponding to levels 0 and 3, respectively) have no impact on the capacitor voltages due to the fact that no current flows through the capacitors. Levels 1 and 2 always have impacts on capacitor voltages. The impacts are different for different redundant switching states and also depend on the direction of phase current. For level 1, if the redundant switching state 1A is employed and $i_k > 0$, the capacitor C_{k2} discharges and V_{Ck2} decreases, and if $i_k < 0$, the capacitor C_{k2} charges and V_{Ck2} increases, while there is no impact on capacitor C_{k1}, as shown in Fig. 2(b). If the redundant switching state 1B is employed, both the capacitor C_{k1} and C_{k2} charge and capacitor voltage V_{Ck1} and V_{Ck2} increase when $i_k > 0$, and both C_{k1} and C_{k2} discharge and V_{Ck1} and V_{Ck2} decrease when $i_k < 0$, as shown

TABLE II
BEHAVIOR OF FC VOLTAGES UNDER DIFFERENT PHASE SWITCHING STATES AND PHASE CURRENTS

Phase voltage, v_k	Output level, L_k	Phase current, i_k	The behavior of flying capacitor voltages	
			V_{Ck1}	V_{Ck2}
$V_{\rm dc}/2$	3	-	No change	No change
$V_{\rm dc}/6$	2	>0	Decrease (2A), Increase (2B)	Decrease (2A), No change (2B)
		<0	Increase (2A), Decrease (2B)	Increase (2A), No change (2B)
$-V_{\rm dc}/6$	1	>0	No change (1A), Increase (1B)	Decrease (1A), Increase (1B)
		<0	No change (1A), Decrease (1B)	Increase (1A), Decrease (1B)
$-V_{\rm dc}/2$	0	-	No change	No change

in Fig. 2(c). A similar analysis can be applied to level 2 as shown in Fig. 2(d) and (e) for the redundant switching states 2A and 2B.

Table II summarizes the behaviors of FC voltages under different switching states and phase currents. As analyzed above, levels 0 and 3 have no impact on V_{Ck1} and V_{Ck2}, while level 1 (with redundant switching state 1A and 1B) and level 2 (with redundant switching state 2A and 2B) have different impacts on V_{Ck1} and V_{Ck2} depending on the selected switching state and the direction of phase current.

III. PROPOSED CAPACITOR VOLTAGE-BALANCING METHOD

A. Algorithm of the Proposed Method

If there is no control on the voltages of the FCs in the NNPC converter, the FC voltages will deviate from their desired value, and this is because there is no control over the currents that flow into/out from the capacitors. The difference between the actual FC voltage and the desired value ($V_{\rm dc}/3$) can be defined as voltage deviation of the FC and can be expressed as

$$\Delta V_{Cki} = V_{Cki} - V_{\rm dc}/3 \tag{2}$$

where V_{Cki} are the capacitor voltages and ΔV_{Cki} are the deviations of the capacitor voltages, $k = a, b, c$, and $i = 1, 2$.

To achieve capacitor voltage balancing, ΔV_{Cki} should be controlled close to zero. If $\Delta V_{Cki} > 0$, the switching state that makes the capacitor voltage decrease should be selected, whereas if $\Delta V_{Cki} < 0$, the switching state that makes the capacitor voltage increase should be selected. However, there is a difficulty in implementing the above principle since the two capacitors in an inverter leg are coupled (charged/discharged jointly) as shown in Table II. For example, assuming that the inverter output voltage is at level 2 ($L_k = 2$), the inverter phase current is positive ($i_k > 0$), the deviation on the capacitor voltage V_{Ck1} is positive ($\Delta V_{Ck1} > 0$), and the deviation on the capacitor voltage V_{Ck2} is negative ($\Delta V_{Ck2} < 0$), the selection of switching state 2A will help to reduce V_{Ck1}, but this selection will make V_{Ck2} to decrease further, which is not desirable. Alternatively, the selection of switching state 2B will help to stop decreasing V_{Ck2}, but will make V_{Ck1} to increase further, which is not desirable either. The coupling of the two capacitors is inherently determined by the converter topology and cannot be eliminated.

TABLE III
LOGIC TABLE FOR BALANCING CAPACITOR VOLTAGE V_{Ck1}

Input Conditions			Output Results
L_k	ΔV_{Ck1}	i_k	The selected switching state (S_k) for controlling V_{Ck1}
2	<0	<0	2A
		≥ 0	2B
	≥ 0	<0	2B
		≥ 0	2A

TABLE IV
LOGIC TABLE FOR BALANCING CAPACITOR VOLTAGE V_{Ck2}

Input Conditions			Output Results
L_k	ΔV_{Ck2}	i_k	The selected switching state (S_k) for controlling V_{Ck2}
1	<0	<0	1A
		≥ 0	1B
	≥ 0	<0	1B
		≥ 0	1A

An effective method for the controlling of the capacitor voltages is proposed by dividing the switching states and capacitors into two groups. As can be seen from Table II, no matter which direction the inverter phase current is, the redundant switching states 2A and 2B always have opposite impact on capacitor voltage V_{Ck1}, while the switching states 1A and 1B always have opposite impact on capacitor voltage V_{Ck2}. Based on this analysis, the switching states 2A and 2B and the capacitor voltage V_{Ck1} are classified as a group. The switching states 1A and 1B and the capacitor voltage V_{Ck2} are classified as the other group. With considering these two groups, Tables III and IV are developed for capacitor voltage-balancing control.

Table III shows the logic table for controlling capacitor voltage V_{Ck1}. The following cases are listed in the table:

1) if $\Delta V_{Ck1} < 0$, the switching state 2A should be selected if $i_k < 0$; otherwise, the switching state 2B is employed if $i_k < 0$;
2) if $\Delta V_{Ck1} \geq; 0$, the switching state 2B should be selected if $i_k < 0$; otherwise, the switching state 2A is employed if $ik \geq; 0$.

In this condition, the capacitor voltage V_{Ck1} is completely controllable regardless of the direction of the inverter phase current.

Table IV shows the logic table for controlling capacitor voltage V_{Ck2}. Similar to Table III, the following cases are listed:

1) if $\Delta; V_{Ck2} < 0$, the switching state 1A should be selected if $i_k < 0$; otherwise, the switching state 1B is employed if $i_k \geq; 0$;
2) if $\Delta; V_{Ck2} \geq; 0$, the switching state 1B should be selected if $i_k < 0$; otherwise, the switching state 1A is employed if $i_k \geq; 0$.

In this condition, the capacitor voltage V_{Ck2} is completely controllable regardless of the direction of the inverter phase current.

TABLE V
SIMPLIFIED LOGIC TABLE FOR BALANCING CAPACITOR VOLTAGE V_{Ck1}

Input Conditions		Output Results
L_k	$\Delta V_{Ck1} \times i_k$	The selected switching state (S_k) for controlling V_{Ck1}
2	<0	2B
	≥ 0	2A

TABLE VI
SIMPLIFIED LOGIC TABLE FOR BALANCING CAPACITOR VOLTAGE V_{Ck2}

Input Conditions		Output Results
L_k	$\Delta V_{Ck2} \times i_k$	The selected switching state (S_k) for controlling V_{Ck2}
1	<0	1B
	≥ 0	1A

The inverter output voltage will switch among voltage levels 0, 1, 2, and 3 in a fundamental period. According to Tables III and IV, V_{Ck2} is under control during level 1, while V_{Ck1} is under control during level 2. In a fundamental period, the capacitor voltages V_{Ck1} and V_{Ck2} are under full control alternately. It should be noted that if the inverter operates at voltage level 1 or level 2 for a long period of time, e.g., at very low fundamental frequencies, the capacitor coupling will cause high ripple on capacitor voltages and a large capacitor is required to suppress the ripple. This issue will be analyzed further in Section IV.

The logic tables in Tables III and IV could be further simplified. The simplified tables are given in Tables V and VI. In this case, $\Delta V_{Cki} \times i_k$ is used as input variable and the logic is simplified into two cases for each table. $\Delta V_{Cki} \times i_k$ could also be replaced by $\mathrm{sign}(\Delta V_{Cki}) \times \mathrm{sign}(i_k)$ and the operator "$\times$" could be processed with logical operation.

As can be seen from Tables V and VI (or Tables III and IV), only the directions of phase current and voltage deviations are required to determine which switching state should be selected and applied to the inverter. This method needs very few computations and is easy to implement.

B. Integration With Different PWM Schemes

The proposed capacitor voltage-balancing method is suitable for and can be easily integrated with different PWM schemes. The schematic diagram for integration is shown in Fig. 3, which could be summarized into the following four steps:

1) first, the output voltage level L_k can be generated by different PWM schemes, such as SPWM, SVM, etc.;
2) the voltage deviation ΔV_{Ck1} and ΔV_{Ck2} should be calculated by (2), and also, the direction of the phase current i_{k} should be determined;
3) Tables V and VI are employed to determine the best redundant switching state out of 1A, 1B and 2A, 2B;
4) finally, the gating signals are generated and applied to power semiconductors.

This procedure indicates that the proposed capacitor voltage-balancing method can be easily integrated with different modulation schemes, and it is simple and easy to implement.

IV. SIMULATION RESULTS

To verify the proposed capacitor voltage-balancing method, simulation studies have been done by using MATLAB/Simulink. Simulation parameters are shown in Table VII. Modulation index m_{a} used in this paper is given by (3), in which V_{ref} is the given peak phase voltage reference, and V_{dc} is dc bus voltage

$$m_a = \sqrt{3} V_{\mathrm{ref}} / V_{\mathrm{dc}} \tag{3}$$

Two PWM schemes, SPWM and SVM, integrated with the proposed capacitor voltage-balancing method, have been studied in both steady state and transient state.

Fig. 4 illustrates the simulation results of the NNPC inverter with SPWM and the proposed voltage-balancing method. Results for two modulation indexes are presented, with $m_a = 0.8$ when $t < 0.1$ s, and $m_a = 0.5$ when $t > 0.1$ s. The line–line voltage, phase current, and six FC voltages are shown in Fig. 4. All the FC voltages are balanced at $V_{\mathrm{dc}}/3$ (1961 V).

Fig. 5 shows the simulation results of NNPC inverter when SVM and the proposed voltage-balancing method are applied, with $m_a = 0.8$ when $t < 0.1$ s, and $m_a = 0.5$ when $t > 0.1$ s. Results similar to the case of SPWM are achieved. FC voltages are balanced at $V_{\mathrm{dc}}/3$ (1961 V).

Dynamic processes of the FC voltages are also investigated and shown in Fig. 6 for SPWM scheme and in Fig. 7 for SVM scheme with the proposed voltage-balancing method. At the beginning (before $t < 0.1$ s), voltage-balancing control is applied and the FC voltages are balanced. At $t = 0.1$ s, the capacitor voltage-balancing control is deactivated, and an artificial discharge of the six FCs is applied, which makes the capacitor voltages start to decrease. During the artificial discharge, the redundant switching states that will discharge FCs are always selected. For example, when $i_k \geq; 0$, the switching state 1A or 2A is selected while when $i_k < 0$ the switching state 1B or 2B is selected. At $t = 0.13$ s, the voltage-balancing method is activated again. Then, the capacitor voltages start to increase under the control of the voltage-balancing method and finally balance at the rated value. These studies verify the effectiveness of the proposed method.

Four different initial capacitor voltage unbalances have been studied to verify the ability of the voltage-balancing method. The results with $m_a = 0.8$ are shown in Fig. 8. The four initial unbalance conditions are $V_{Ca1} = V_{Ca2} = V_{\mathrm{dc}}/2$ [see Fig. 8(a)], $V_{Ca1} = V_{Ca2} = 0$ [see Fig. 8(b)], $V_{Ca1} = V_{\mathrm{dc}}/2$ and $V_{Ca2} = 0$ [see Fig. 8(c)], and $V_{Ca1} = 0$ and $V_{Ca2} = V_{\mathrm{dc}}/2$ [see Fig. 8(d)]. The results show that the capacitor voltages can come to balance in each case.

As previously analyzed, the two capacitors in a leg of the NNPC inverter are coupled. The coupling will bring some limitations to the inverter in some applications in terms of the capacitor size. To demonstrate the limitation, the NNPC inverter has been investigated under different fundamental frequencies and load power factors for two types of commonly used motor loads. The first is the fan/pump type of loads, where the electromagnetic torque of the motor is proportional to the square of the rotor speed. The second type is the constant torque load,

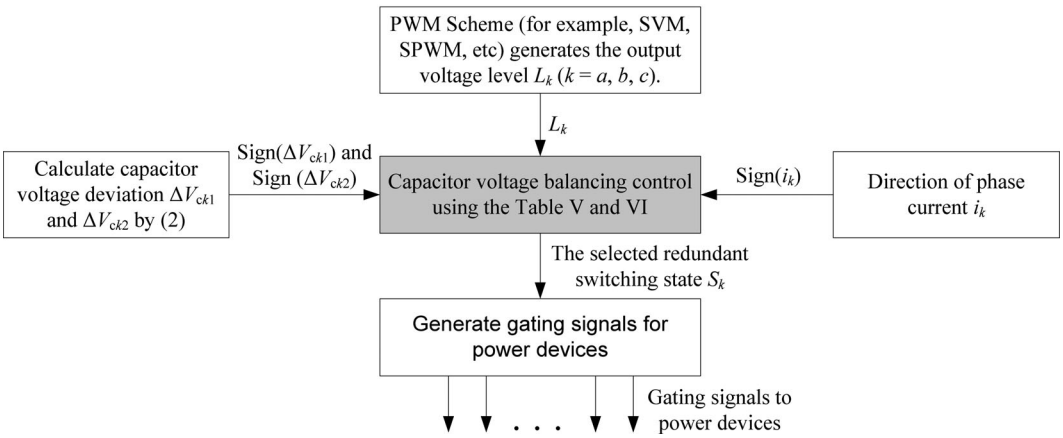


Fig. 3. Schematic diagram for integration of the proposed capacitor voltage-balancing method with PWM schemes.

TABLE VII
SIMULATION PARAMETERS

Simulation Parameters	Values
Output Power	1 MVA
Output Voltage	4160 V
Flying Capacitors	819 μF (5.3 p.u.)
Switching Frequency	700 Hz
DC Bus Voltage	5883 V
Fundamental Frequency	60 Hz
Load Inductance	24.42 mH
Load Resistance	14.65 Ω

where the torque is nearly constant over the full speed range. In variable-speed drives, the inverter output voltage is approximately proportional to its fundamental frequency to keep the rotor flux constant. In the case of fan/pump type of loads, the inverter output current is proportional to the square of the fundamental frequency, whereas for the constant torque load, the inverter output current is kept nearly constant in the full speed range.

The operation of the inverter at different fundamental frequencies and load power factors have been investigated by simulation for the two types of loads, and FCs are sized to keep the peak-to-peak capacitor voltage ripple within 15%. The switching frequency is 700 Hz for both cases. Under these conditions, the required capacitor sizes in per unit (p.u.) are given in Fig. 9(a) and (b) for fan/pump and constant torque types of loads, respectively. As can be seen from Fig. 9(a), the required capacitor size for fan/pump types of loads increases with the fundamental frequency, so the capacitor should be sized by the value at the highest (rated) operating frequency. For the constant torque loads as shown in Fig. 9(b), the results are opposite. The required capacitor size decreases with the increase of fundamental frequency, so the capacitor should be sized according to the lowest operating frequency.

It is obvious from Fig. 9 that with the constant torque load, the inverter needs a very large capacitor value (over 30 p.u.) to keep their voltage ripple within 15%, which limits the NNPC inverter for this type of applications. However, for the fan/pump type of loads, the inverter works well without the need of large capacitance. A 4.8–p.u. capacitance can keep the peak-to-peak capacitor voltage ripple within 15% in the full speed range.

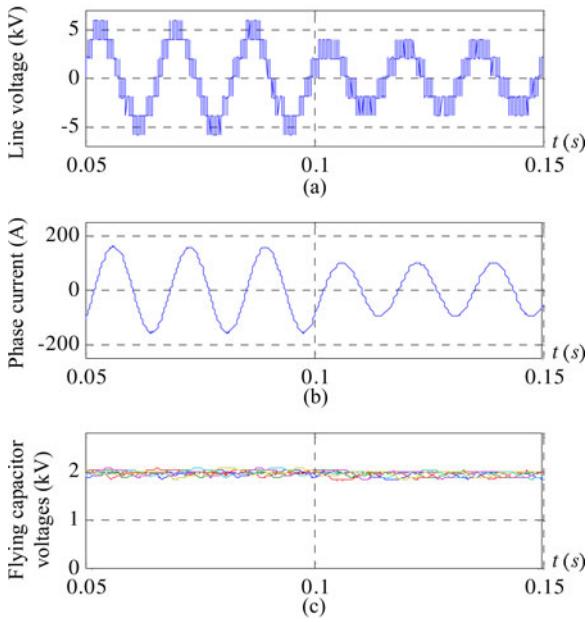


Fig. 4. Simulation results of NNPC inverter with SPWM and the voltage-balancing method for $m_a = 0.8$ ($t < 0.1$ s) and $m_a = 0.5$ ($t > 0.1$ s). (a) Line–line voltage. (b) Phase current. (c) Six FC voltages.

V. EXPERIMENTAL RESULTS

Experiments are carried out to verify the feasibility of the proposed method. The parameters of Table VIII are used for experimental setup as a scaled-down prototype.

Fig. 10 shows the experimental results of the NNPC inverter with SPWM and the voltage-balancing method. Fig. 11 shows the experimental results of the NNPC inverter with SVM and the voltage-balancing method. For each case, the line–line voltage, three-phase currents, and four FC voltages (V_{Ca1}, V_{Ca2}, V_{Cb1}, and V_{Cb2}) are presented. Results for two different modulation

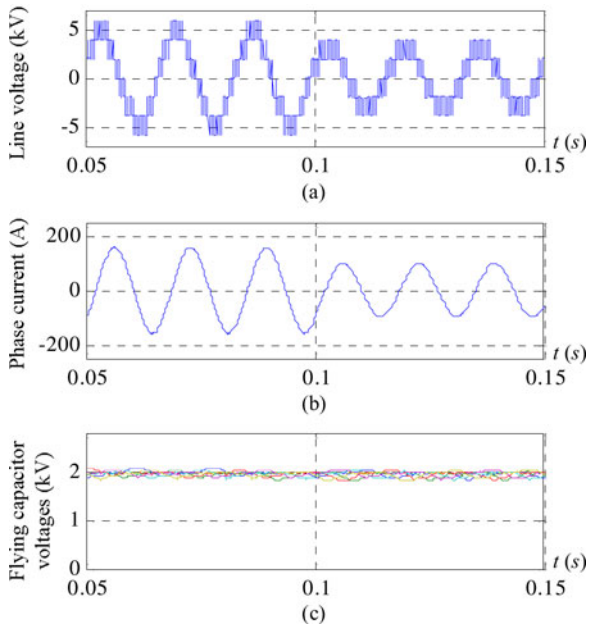


Fig. 5. Simulation results of NNPC inverter with SVM and the voltage-balancing method for $m_a = 0.8$ ($t < 0.1$ s) and $m_a = 0.5$ ($t > 0.1$ s). (a) Line–line voltage. (b) Phase current. (c) Six FC voltages.

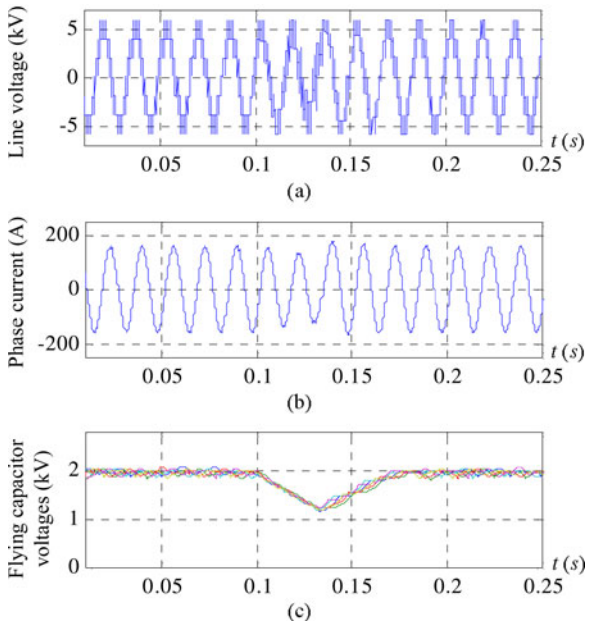


Fig. 7. Simulation results of NNPC inverter with and without the capacitor voltage-balancing control under SVM scheme. (a) Line–line voltage. (b) Phase current. (c) Six FC voltages.

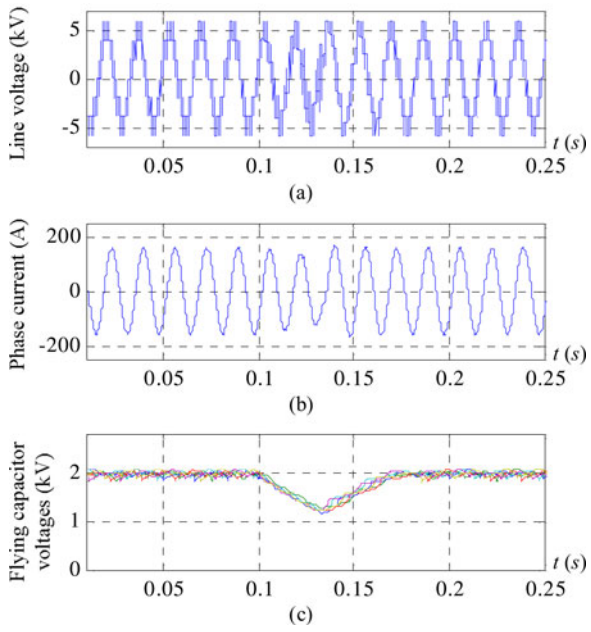


Fig. 6. Simulation results of NNPC inverter with and without the capacitor voltage-balancing control under SPWM scheme. (a) Line–line voltage. (b) Phase current. (c) Six FC voltages.

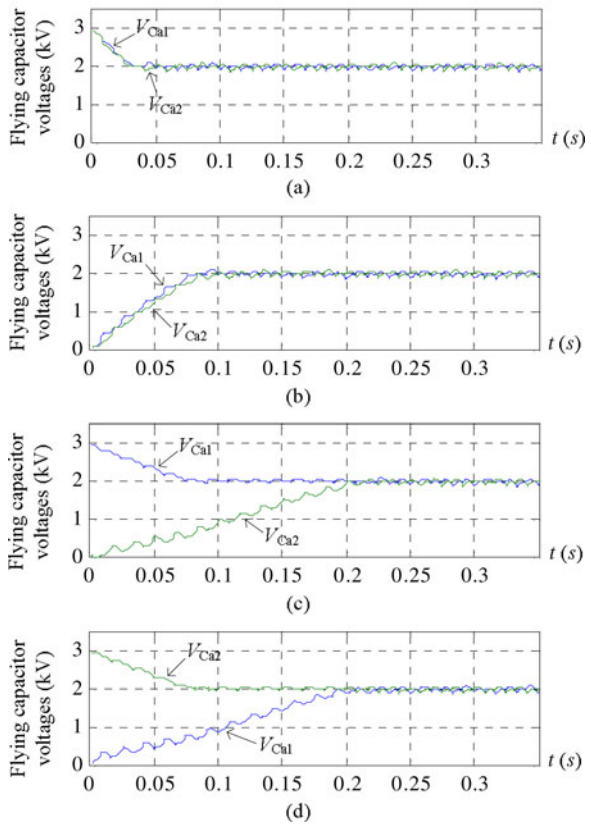


Fig. 8. Capacitor voltages of V_{Ca1} and V_{Ca2} starting with different initial voltage unbalances ($m_a = 0.8$). (a) $V_{Ca1} = V_{Ca2} = V_{\rm dc}/2$. (b) $V_{Ca1} = V_{Ca2} = 0$. (c) $V_{Ca1} = V_{\rm dc}/2$ and $V_{Ca2} = 0$. (d) $V_{Ca1} = 0$ and $V_{Ca2} = V_{\rm dc}/2$.

indexes, $m_a = 0.8$ and $m_a = 0.5$, are shown respectively. As can be seen from Figs. 10 and 11, all the FC voltages are well balanced.

Experimental results for dynamic processes of the FC voltages are given in Figs. 12 and 13 for SPWM and SVM, respectively. For each case, the process is divided into three

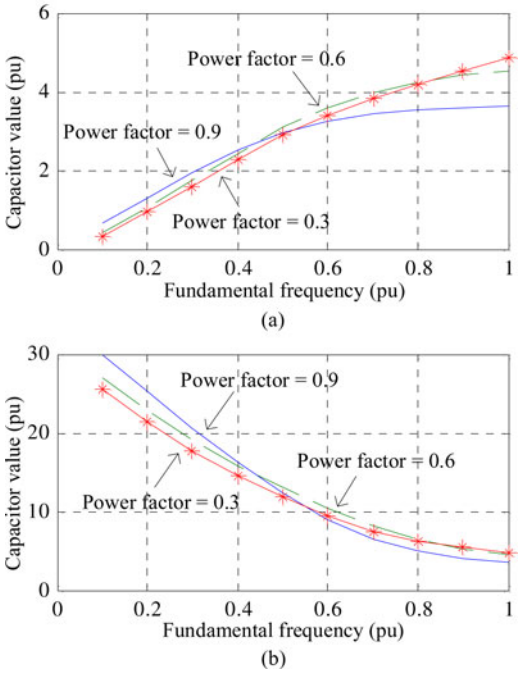


Fig. 9. FC value versus the inverter fundamental frequency with maximum peak-to-peak capacitor voltage ripple of 15%. (a) Fan/pump type of loads. (b) Constant torque type of loads.

TABLE VIII
EXPERIMENTAL PARAMETERS

Experimental Parameters	Values
Output Power	6350 VA
Output Voltage	212 V
Flying Capacitors	2000 μF (5.3 p.u.)
Switching Frequency	700 Hz
DC Bus Voltage	300 V
Fundamental Frequency	60 Hz
Load Inductance	10 mH
Load Resistance	6 Ω

stages, as indicated by Stages I, II, and III in Figs. 12 and 13. At Stage I, the voltage-balancing method is applied and FC voltages are balanced. At Stage II, the voltage-balancing method is deactivated and the FC voltages are artificially decreased to about 60% of the rated value. At Stage III, the voltage-balancing method is activated again. The FC voltages start to recover and finally balance at rated value. The experimental results verify the effectiveness of the proposed method.

VI. CONCLUSION

A capacitor voltage-balancing method for a four-level NNPC inverter is proposed in this paper. The proposed method takes advantage of redundancy in phase switching states to control and balance the FC voltages. Simple and effective logic tables are developed for the balancing control. The method is easy to implement and needs very few computations. Moreover, the

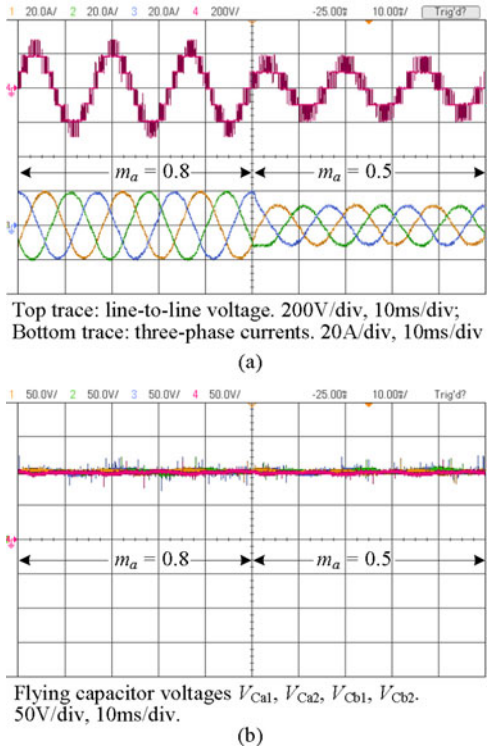


Fig. 10. Experimental results of NNPC inverter with SPWM and the voltage-balancing method for $m_a = 0.8$ and $m_a = 0.5$. (a) Line–line voltage and three-phase currents. (b) Capacitor voltages V_{Ca1}, V_{Ca2}, V_{Cb1}, and V_{Cb2}.

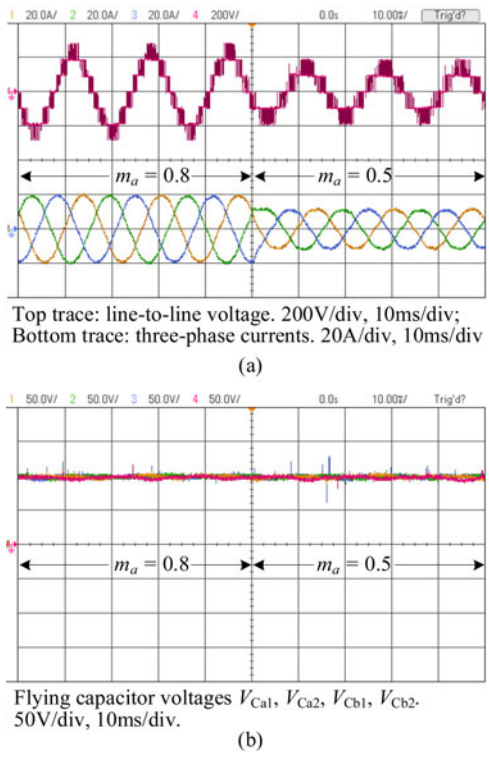
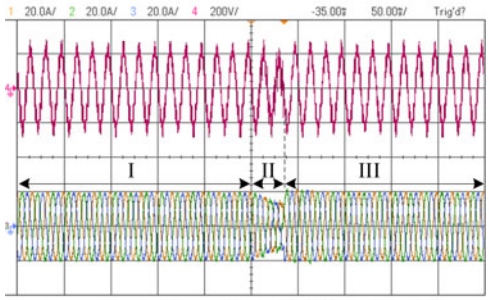
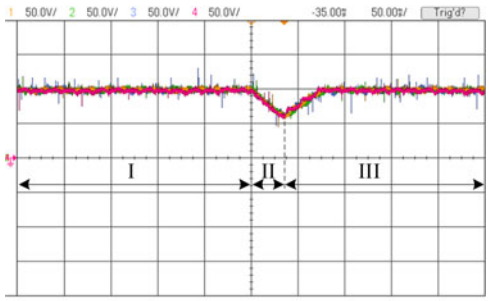


Fig. 11. Experimental results of NNPC inverter with SVM and the voltage-balancing method for $m_a = 0.8$ and $m_a = 0.5$. (a) Line–line voltage and three-phase currents. (b) Capacitor voltages V_{Ca1}, V_{Ca2}, V_{Cb1}, and V_{Cb2}.



Top trace: line-to-line voltage. 200V/div, 50ms/div;
Bottom trace: three-phase currents. 20A/div, 50ms/div

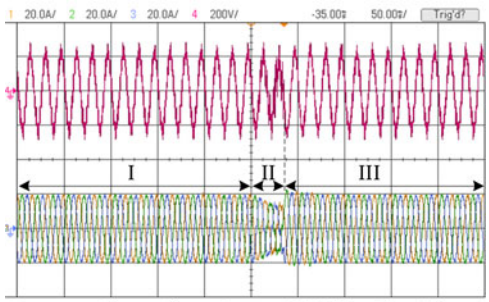
(a)



Flying capacitor voltages V_{Ca1}, V_{Ca2}, V_{Cb1}, V_{Cb2}.
50V/div, 50ms/div.

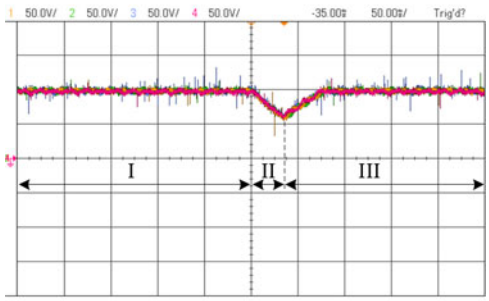
(b)

Fig. 12. Experimental results of NNPC inverter with and without the capacitor voltage-balancing control under SPWM scheme. (a) Line–line voltage and three-phase currents. (b) Capacitor voltages V_{Ca1}, V_{Ca2}, V_{Cb1}, and V_{Cb2}.



Top trace: line-to-line voltage. 200V/div, 50ms/div;
Bottom trace: three-phase currents. 20A/div, 50ms/div

(a)



Flying capacitor voltages V_{Ca1}, V_{Ca2}, V_{Cb1}, V_{Cb2}.
50V/div, 50ms/div.

(b)

Fig. 13. Experimental results of NNPC inverter with and without the capacitor voltage-balancing control under SVM scheme. (a) Line–line voltage and three-phase currents. (b) Capacitor voltages V_{Ca1}, V_{Ca2}, V_{Cb1}, and V_{Cb2}.

method is suitable for and easy to integrate with different PWM schemes. The limitation of the NNPC inverter in terms of the voltage balancing and capacitor size is also investigated. The effectiveness and feasibility of the proposed method is verified by simulation and experimental results.

REFERENCES

[1] B. Wu, *High-Power Converters and AC Drives.* New York, NY, USA: Wiley/IEEE Press, 2006, ch. 1.

[2] N. Mittal, B. Singh, S. P. Singh, R. Dixit, and D. Kumar, "Multilevel inverters: A literature survey on topologies and control strategies," in *Proc. 2nd Int. Conf. Power, Control Embedded Syst.*, 2012, pp. 1–11.

[3] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[4] R. Stala, "A natural dc-link voltage balancing of diode-clamped inverters in parallel systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 5008–5018, Nov. 2013.

[5] J. Mei, K. Shen, B. Xiao, L. M. Tolbert, and J. Zheng, "A new selective loop bias mapping phase disposition PWM with dynamic voltage balance capability for modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 798–807, Feb. 2014.

[6] M. Narimani, B. Wu, Z. Cheng, and N. Zargari, "A new nested neutral point clamped (NNPC) converter for medium-voltage (MV) power conversion," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 5259–5270, Dec. 2014.

[7] A. Choudhury, P. Pillay, and S. S. Williamson, "DC-link voltage balancing for a three-level electric vehicle traction inverter using an innovative switching sequence control scheme," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 2, pp. 296–307, Jun. 2014.

[8] Z. Shu, N. Ding, J. Chen, H. Zhu, and X. He, "Multilevel SVPWM With dc-link capacitor voltage balancing control for diode-clamped multilevel converter based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1884–1896, May 2013.

[9] S. Busquets-Monge, S. Alepuz, J. Bordonau, and J. Peracaula, "Voltage balancing control of diode-clamped multilevel converters with passive front-ends," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1751–1758, Jul. 2008.

[10] S. Busquets-Monge, R. Maheshwari, and S. Munk-Nielsen, "Overmodulation of n-Level three-leg dc-ac diode-clamped converters with comprehensive capacitor voltage balance," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1872–1883, May 2013.

[11] A. H. Bhat and N. Langer, "Capacitor voltage balancing of three-phase neutral-point-clamped rectifier using modified reference vector," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 561–568, Feb. 2014.

[12] J. Pou, R. Pindado, and D. Boroyevich, "Voltage-balance limits in four-level diode-clamped converters with passive front ends," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 190–196, Feb. 2005.

[13] P. Chaturvedi, S. Jain, and P. Agarwal, "Carrier-based neutral point potential regulator with reduced switching losses for three-level diode-clamped inverter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 613–624, Feb. 2014.

[14] M. Khazraei, H. Sepahvand, K. Corzine, and M. Ferdowsi, "A generalized capacitor voltage balancing scheme for flying capacitor multilevel converters," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2010, pp. 58–62.

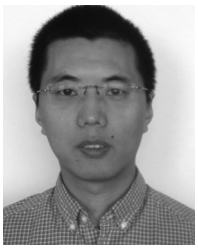
[15] M. Khazraei, H. Sepahvand, K. A. Corzine, and M. Ferdowsi, "Active capacitor voltage balancing in single-phase flying-capacitor multilevel power converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 769–778, Feb. 2012.

[16] B. P. McGrath and D. G. Holmes, "Natural capacitor voltage balancing for a flying capacitor converter induction motor drive," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1554–1561, Jun. 2009.

[17] A. M. Y. M. Ghias, J. Pou, M. Ciobotaru, and V. G. Agelidis, "Voltage-balancing method using phase-shifted PWM for the flying capacitor multilevel converter," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4521–4531, Sep. 2014.

[18] S. Thielemans, T. J. Vyncke, and J. Melkebeek, "Weight factor selection for model-based predictive control of a four-level flying-capacitor inverter," *IET Power Electron.*, vol. 5, no. 3, pp. 323–333, 2012.

[19] S. Choi and M. Saeedifard, "Capacitor voltage balancing of flying capacitor multilevel converters by space vector PWM," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1154–1161, Jul. 2012.
[20] E. Solas, G. Abad, J. A. Barrena, S. Aurtenetxea, A. Carcar, and L. Zajac, "Modular multilevel converter with different submodule concepts—Part I: Capacitor voltage balancing method," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4525–4535, Oct. 2013.
[21] M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel PWM inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1786–1799, Jul. 2010.
[22] M. Hagiwara and H. Akagi, "Control and experiment of pulse width-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.
[23] M. Narimani, V. Yaramasu, B. Wu, G. Cheng, and N. Zargari, "Model predictive control of nested neutral point clamped (NNPC) converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 1174–1179.
[24] M. Narimani, B. Wu, V. Yaramasu, Z. Cheng, and N. Zargari, "Finite control-set model predictive control (FCS-MPC) of nested neutral point clamped (NNPC) converter," *IEEE Trans. Power Electron.*, 2015, early access.
[25] K. Tian, B. Wu, M. Narimani, D. Xu, Z. Cheng, and N. Zargari, "A space vector modulation method for common-mode voltage reduction in nested neutral point clamped inverter," in *Proc. 40th Annu. Conf. IEEE Ind. Electron. Soc.*, 2014, pp. 4541–4547.



Kai Tian received the B.Sc., M.A.Sc., and Ph.D. degrees in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2004, 2006, and 2010, respectively.

He is currently a Postdoctoral Research Associate at the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada. He is the author of more than 15 journal and conference papers. He holds four U.S./European granted/pending patents in power converters and medium voltage applications. His current research interests include power conversion and medium-voltage drives.

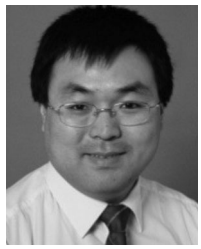
Bin Wu (S'89–M'92–SM'99–F'08) received the M.A.Sc. and Ph.D. degrees in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 1989 and 1993, respectively.

He joined Ryerson University, Toronto, in 1993, where he is currently a Professor and Senior NSERC/Rockwell Automation Industrial Research Chair in Power Electronics and Electric Drives. His has published more than 300 technical papers, authored/coauthored two Wiley-IEEE Press books, and holds more than 25 granted/pending U.S./European patents in the area of power conversion, medium-voltage drives, and renewable energy systems.

Dr. Wu received the Gold Medal of the Governor General of Canada in 1993, Premier's Research Excellence Award in 2001, NSERC Synergy Award for Innovation in 2002, Ryerson Distinguished Scholar Award in 2003, YSGS Outstanding Contribution to Graduate Education Award, and Professional Engineers Ontario Engineering Excellence Medal in 2014. He is a Fellow of Engineering Institute of Canada and Canadian Academy of Engineering.

Mehdi Narimani (S'09–M'13–SM'15) received the B.S. and M.S. degrees from the Isfahan University of Technology, Isfahan, Iran, in 1999 and 2002, respectively, and the Ph.D. degree from the University of Western Ontario, London, ON, Canada, all in electrical engineering.

He is currently a Postdoctoral Research Associate at the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada, and Rockwell Automation Canada. He was a Faculty Member of the Isfahan University of Technology from 2002 to 2009, where he was involved in design and implementation of several industrial projects. He is the author of more than 50 journal and conference proceeding papers and four patents (pending review). His current research interests include high-power converters, control of power electronics, and renewable energy systems.



Dewei (David) Xu (S'99–M'01) received the B.Sc., M.A.Sc., and Ph.D. degrees in electrical engineering from Tsinghua University, Beijing, China, in 1996, 1998, and 2001, respectively.

Since 2001, he has been with Ryerson University, Toronto, ON, Canada, where he is currently an Associate Professor. His research interests include renewable energy systems, high-power converters, electric motor drives, and advanced digital control for power electronics.

Zhongyuan Cheng received the M.A.Sc. degree in electrical and computer engineering from Ryerson University, Toronto, ON, Canada, in 2005, and the Ph.D. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 1995.

In 2006, he joined Rockwell Automation Canada, Cambridge, ON, Canada. He is currently working on medium-voltage drive topologies, power electronics design, and motor drive control. His research interests include new converter topologies: control/performance analysis and component sizing for high-power medium-voltage drives; the integration and applications of medium-voltage industrial drives: drive-utility interactions; the application of MV drives in generator systems; and drive stability issues in special applications.

Navid Reza Zargari (M'94–SM'08–F'15) received the B.Eng. degree from Tehran University, Tehran, Iran, in 1987, and the M.A.Sc. and Ph.D. degrees from Concordia University, Montreal, QC, Canada, in 1991 and 1995, respectively.

He has been with Rockwell Automation Canada, Cambridge, ON, Canada, since November 1994, first as a Senior Designer, then as the Manager of the Medium-Voltage R&D Department and currently as a Product Architect. For the past 19 years, he has been involved with simulation, analysis, and design of power converters for medium-voltage ac drives. His research interests include power converter topologies and their control aspects, power semiconductors, and renewable energy sources. He has coauthored more than 80 research papers as well as a book *Power Conversion and Control of Wind Energy Systems* (New York, NY, USA: Wiley/IEEE Press, 2011). He holds 30 U.S. granted/pending patents in power converters and medium-voltage applications.

Dr. Zargari received the Premier's Award for the Innovator of the year in 2009 from the Province of Ontario.